ABSTRACT OF THE DISCLOSURE

A method and apparatus for utilizing data speculation concurrently with out-of-order instruction execution is disclosed. In one embodiment, a test instruction corresponding to a previously-issued advanced load instruction has a second instance of the logical destination register used by the advanced load appended as a logical source register during a decode stage. When out-of-order register renaming occurs, the appended source register may be mapped to the same physical register as that used in the first instance by the advanced load instruction. This may facilitate the determination of whether or not the results of the advanced load instruction are valid.